an interface circuit configured to control access to said memory, the interface circuit coupled to said memory;

an [i]embedded processor configured to control the integrated circuit, the embedded processor configured to control the interface circuit to receive information therefrom;

an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom; and

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a shared operand unit coupled to the first MAC unit and the second MAC unit for providing a shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other.

2. (Amended) The integrated circuit according to claim 1 wherein said array processor uses a simplified IEEE floating point notation which excludes said IEEE floating point exceptions, comprising underflow, overflow, divide by zero, inexact, and invalid.

[comprises:

a plurality of multiply/accumulators; and

a shared operand circuit coupled to provide a shared operand to at least two of said plurality of multiplier/accumulators.]

(Amended)

3. The integrated circuit according to claim 1 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and the array processor..

4. The integrated circuit according to claim 3 wherein said wire bundle comprises at least 256 wires.

5. (NEW) The integrated circuit according to claim 1 wherein the MAC unit comprises a computational unit that multiplies a first operand by a second operand to obtain a result and then adds or subtracts from the result a third operand, wherein the operands are either scalars or vectors.

6. (NEW) The integrated circuit according to claim 1 further comprising

a global external bus unit for providing an interface between the integrated circuit and the external environment, the global external bus unit coupled to the embedded microprocessor by a system bus and by a separate dedicated bus.

7. (NEW) The integrated circuit according to claim 1 wherein the array processor performs a plurality of vector operations selected from a group consisting of addition of a plurality of vectors and multiplying a vector by a scalar.

8. (NEW) A array processor for frame rendering and DSP applications, comprising:

a first arithmetic unit coupled to a first local memory, the first local memory comprising a first plurality of operands, and the first arithmetic unit performing at least one first single precision floating point operation of addition, subtraction, or multiplication;

a second arithmetic unit coupled to a second local memory, the second local memory comprising a second plurality of operands and the second arithmetic unit performing at least one second single precision floating point operations of addition, subtraction, or multiplication;

a shared operand unit coupled to the first arithmetic unit and the second arithmetic unit for providing a shared operand to both units; and

wherein the first arithmetic unit and the second arithmetic unit execute independently and concurrently.